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A Bridgeless Cuk Converter Fed PMDC Drive for PFC Applications and Reduction in THD Values Using Sinusoidal PWM Technique

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***Abstract* — New bridgeless single-phase ac–dc power factor correction (PFC) rectifiers based on Cuk topology are proposed.The absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each interval of the switching cycle result in less conduction losses and an improved thermal management compared to the conventional Cuk PFC rectifier. The proposed topologies are designed to work in discontinuous conduction mode (DCM) to achieve almost a unity power factor and low total harmonic distortion of the input current. The DCM operation gives additional advantages such as zero-current turn-ON in the power switches, zero-current turn-OFF in the output diode, and simple control circuitry. Performance comparisons between the proposed and conventional Cuk PFC rectifiers are performed based on circuit simulations. Simulation results for a 18W/12Vdc at 120V line voltage to evaluate the performance of the proposed bridgeless PFC rectifiers are obtained.**

***Index Terms*—Bridgeless rectifier, Cuk converter, low conduction losses, power factor correction (PFC), rectifier, single-ended primary-inductor converter (SEPIC) converter, total harmonic distortion (THD), Discontinuous conduction mode (DCM).**

I.INTRODUCTION

POWER supplies with active power factor correction(PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards,such as the IEC 61000-3-2. Most of the PFC rectifiers utilize a boost converter at their front end. However, a conventional PFC scheme has lower efficiency due to significant losses in the diode bridge. A conventional PFC Cuk rectifier is shown in Fig. 1; the current flows through two rectifier bridge diodes and the power switch (Q) during the switch ON-time, and through two rectifier bridge diodes and the output diode (Do) during the switch OFF-time. Thus, during each switching cycle, the current flows through three power semiconductor devices. As a result, a significant conduction loss, caused by the forward voltage drop across the bridge diode, would degrade the converter's efficiency. In an effort to maximize the power supply efficiency, the number of semiconductors generating losses is reduced by essentially eliminating the full bridge input diode rectifier.

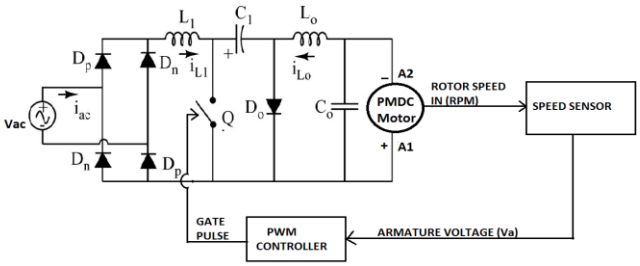


Fig.1.Conventional Cuk PFC Converter.

A bridgeless PFC rectifier allows the current to flow through a minimum number of switching devices compared to the conventional PFC rectifier. Accordingly,the converter conduction losses can be significantly reduced and higher efficiency can be obtained, as well as cost savings. Recently, several bridgeless PFC rectifiers have been introduced to improve the rectifier power density and/or reduce noise emissions via soft-switching techniques or coupled magnetic topologies [1]–[5].On the other hand, the bridgeless boost rectifier [7]–[24] has the same major practical drawbacks as the conventional boost converter such as the dc output voltage is higher than the peak input voltage, lack of galvanic isolation, and high start-up inrush currents. Therefore, for low-output voltage applications, such as telecommunication or computer industry, an additional converter or an isolation transformer is required to step-down the voltage.

To overcome these drawbacks, several bridgeless topologies which are suitable for step-up/step-down applications have been recently introduced. However, the proposed topology in still suffers from having three semiconductors in the current conduction path during each switching cycle. Similar to the boost converter, the SEPIC converter has the disadvantage of discontinuous output current resulting in a relatively high output ripple. A bridgeless buck PFC rectifier was recently proposed for step-down applications. However, the input line current cannot follow the

input voltage around the zero crossings of the input line voltage; besides, the output to input voltage ratio is limited to half. Also, buck PFC converter results in an increased total harmonic distortion (THD) and a reduced power factor.

II. PROPOSED BRIDGELESS CUK PFC RECTIFIERS

The Cuk converter offers several advantages in PFC applications,such as easy implementation of transformer isolation,natural protection against inrush current occurring at start-up or overload current, lower input current ripple, and less electromagnetic interference (EMI) associated with the discontinuous conduction mode (DCM) topology. Unlike the SEPIC converter, the Cuk converter has both continuous input and output currents with a low current ripple. Thus, for applications,which require a low current ripple at the input and output ports of the converter, the Cuk converter seems to be a potential candidate in the basic converter topologies.In this paper, three topologies of bridgelessCuk PFC rectifiers are proposed. The proposed rectifiers are compared based on efficiency, components count, harmonics, gain capability, and driver circuit.

The proposed bridgeless Cuk PFC rectifiers are shown in Fig.2.The proposed topologies are formed by connecting two dc–dc Cuk converters, one for each half-line period (T/2) of the input voltage. It should be mentioned here that the topology of Fig.3(a) was listed as a new converter topology. The operational circuits during the positive and negative half-line period for the proposed bridgeless Cuk rectifiers of Fig. 3(a)–(b) are shown in Fig. 3 respectively. Note that by referring to Fig.3,there are one or two semiconductor(s) in the current flowing path; hence, the current stresses in the active and passive switches are further reduced and the circuit efficiency is improved compared to the conventional Cuk rectifier. In addition, Fig. 3(a) and (b) shows that one rail of the output voltage bus is always connected to the input ac line through the slow-recovery diodes Dp and Dn or directly as in the case of the topology of Fig. 3(b). Thus, the proposed topologies do not suffer from the high common-mode EMI noise emission problem and have common-mode EMI performance similar to the conventional PFC topologies. Consequently, the proposed topologies appear to be promising candidates for commercial PFC products.

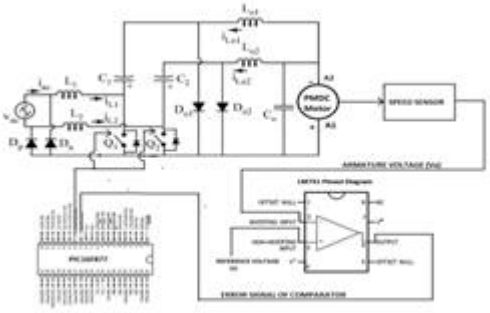


Fig. 2. Proposed bridgeless Cuk PFC rectifiers.

The proposed bridgeless rectifiers of Fig.2 utilize two power switches (Q1 and Q2). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Compared to the conventional Cuk topology, the structure of the proposed topologies utilizes one additional inductor, which is often described as a disadvantage in terms of size and cost. However, a better thermal performance can be achieved with the two inductors compared to a single inductor.It should be mentioned here that the three inductors in the proposed topologies can be coupled on the same magnetic core allowing considerable size and cost reduction. Additionally,the "near zero-ripple-current" condition at the input or output port of the rectifier can be achieved without compromising performance.

III. PRINCIPLE OF OPERATION AND THEORETICAL ANALYSIS

A. Principle of Operation

The proposed bridgeless type Cuk rectifier of Fig.2 will be considered in this study. Type 2 (SEPIC converter) is similar to type 3, except for the output stage stresses. The SEPIC version of type 2 has been analyzed theoretically. The analysis assumes that the converter is operating at a steady state in addition to the following assumptions: pure sinusoidal input voltage, ideal lossless components, and all capacitors are large enough such that their switching voltage ripples are negligible during the switching period Ts. Moreover, the output filter capacitor Co (Co1 and Co2 for topology 2) has a large capacitance such that the voltage across it is constant over the entire line period. Referring to Fig. 3(a), during the positive half-line cycle, the first dc–dc Cuk circuit, L1–Q1–C1–Lo 1–Do1 , is active through diode Dp , which connects the input ac source to the output. During the negative half-line cycle, as shown in Fig. 3(b), the second dc–dc Cuk circuit, L2–Q2 -C2–Lo 2–Do2, is active through diode Dn , which connects the input ac source to the output.Due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half cycle of the input voltage.Moreover, the operation of the proposed rectifiers of Fig.2 will be described assuming that the three inductors are operating in DCM. By operating the rectifier in DCM, several advantages can be gained. These advantages include natural near-unity power factor, the power switches are turned ON at zero current, and the output diodes (Do1 and Do2) are turned OFF at zero current.Thus, the losses due to the turn-ON switching and the reverse recovery of the output diodes are considerably reduced.Conversely, DCM operation significantly increases the conduction losses due to the increased current stress through circuit components. As a result, this leads to one disadvantage of the DCM operation, which limits its use to low-power applications (<300 W) similar to the conventional Cuk converter, the circuit operation in DCM can be divided

into three distinct operating stages during one switching period Ts. Equivalent circuits over a switching period Ts in the positive and negative half-line period of input line voltage is shown in Fig.3(a-b) shows DCM operation of switch over switching cycle during the positive & negative half cycle period of the input voltage.

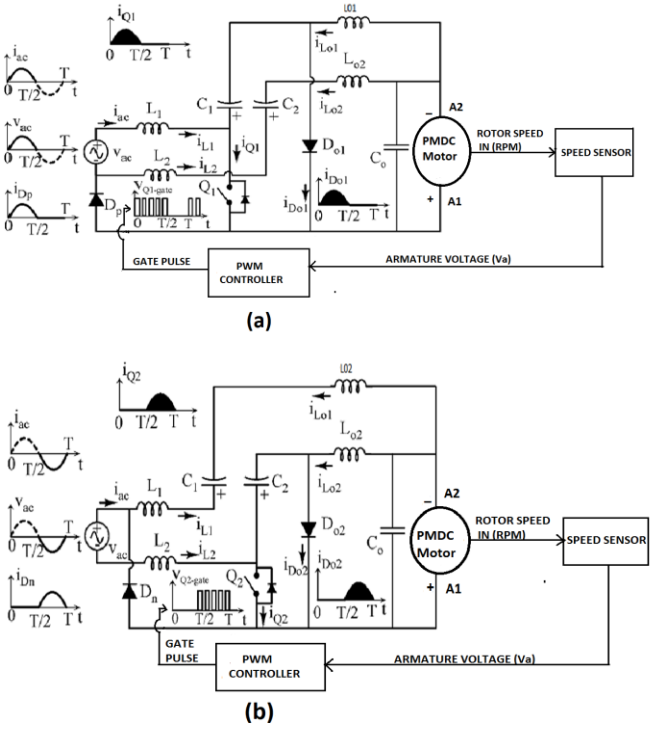


Fig.3.Equivalent circuit of proposed bridgeless PFC Cuk rectifier Fig.3(a) During positive half-line period.Fig.3(b) During negative half- line period of input voltage.

Stage 1[t0, t1], [Fig. 4(a)]: This stage starts when the switch Q1 is turned ON. Diode Dp is forward biased by the inductor current iL1 . As a result, the diode Dn is reverse biased by the input voltage. The output diode Do1 is reverse biased by the reverse voltage (vac + Vo), while Do2 is reverse biased by the output voltage Vo. In this stage, the currents through inductors L1 and Lo1 increase linearly with the input voltage, while the current through Lo2 is zero due to the constant voltage across C2. The inductor currents are given as

$$\frac{di}{dt} = \frac{Vac}{Ln}, n = 1,01 \qquad (1)$$

Accordingly, the peak current through the active switch Q1 is given by

$$IQ1, pk = \frac{Vm}{Le} D1Ts \qquad (2)$$

where Vm is the peak amplitude of the input voltage vac , D1 is the switch duty cycle, and Le is the parallel combination of inductors L1 and Lo1.

Stage 2[t1, t2] [Fig. 4(b)]: This stage starts when the switch Q1 is turned OFF and the diode Do1 is turned ON simultaneously providing a path for the inductor currents iL1 and iLo1. The diode Dp remains conducting to provide a path for iL1. Diode Do2 remains reverse biased during this interval. This interval ends when iDo1 reaches zero and Do1 becomes reverse biased. Note that the diode Do1 is switched OFF at zero current. Similarly,the inductor currents of L1 and Lo1 during this stage can be represented as follows

$$\frac{di}{dt} = -\frac{V0}{Ln}, n = 1,01 \qquad (3)$$

Stage 3[t2, t3] [Fig. 4(c)]: During this interval, only the diode Dp conducts to provide a path for iL1 . Accordingly, the inductors in this interval behave as constant current sources. Hence, the voltage across the three inductors is zero. The capacitor C1 is being charged by the inductor current iL1. This period ends when Q1 is turned ON.

By applying inductor volt-second across L1 and Lo1 , the normalized length of the second stage period can be expressed as follows

. $$D2 = \frac{D1}{M} \sin \omega t \qquad (4)$$

where ω is the line angular frequency, and M is the voltage conversion ratio (M = Vo /Vm).

Since the diode Dp continuously conducts throughout the entire switching period, the average voltage across C2 is equal to the output voltage Vo. As a result, a negligible ac current will flow through C2 and Lo2 . Therefore, the current through L2 during the positive half cycle of the input voltage is equal to the negative current through the body diode of Q2 . It should be noted that the body diode of the inactive switch Q2 is always conducting current during the positive half cycle of the input voltage. This is due to the low impedance of the input inductors (L1 and L2) at the line frequency. Therefore, the input diode Dp and body diode of Q2 appear in parallel configuration to share the return current. A large portion of the return current will pass through the diode that has a lower voltage drop. The efficiency of the converter can be slightly improved by using synchronous rectification to turn ON the switch Q2 during the positive half

cycle of the input voltage, which eliminates its body-diode conduction.

B. Voltage Conversion Ratio M

The voltage conversion ratio M in terms of the converter parameters can be obtained by applying the power balance principle.

Similar to the conventional Cuk PFC rectifier, shows that the input port of the proposed rectifier obeys Ohm's law. Thus, the input current is sinusoidal and in phase with the input voltage. Hence, the power stage circuit of the converter of Fig. 4 can be represented by its large signal averaged model This model can be implemented in a simulation program to predict the steady state and large signal dynamic characteristics of the real circuit. Furthermore, the averaged model can greatly reduce the long computation time when it is implemented in simulation software.

$$M = \frac{V0}{Vm} = \sqrt{\frac{Rl}{2\,\mathrm{Re}}} \qquad (5)$$

It should be noted that the voltage gain is also valid for the other two proposed topologies. However, the effective inductance (Le) varies from one topology to another.

C. Boundaries Between Continuous Conduction Mode and DCM

Referring to the diode Do1 current waveform in Fig.4, the DCM operation mode requires that the sum of the switch duty cycle and the normalized switch-OFF time length be less than one, Hence, the minimum and maximum values of Ke -crit is given by

$$Ke-crit-\min = \frac{1}{2(M+1)^2} \qquad (6)$$

respectively. Therefore, for values of Ke < Ke -crit min, the converter always operates in DCM, and it operates in the continuous conduction mode (CCM) for values of Ke > Ke -crit max. However for values of Ke -crit min < Ke < Ke -crit max, the converter operates in both modes: CCM near the peak value of the input line voltage and DCM near the zero crossing of the input line voltage.

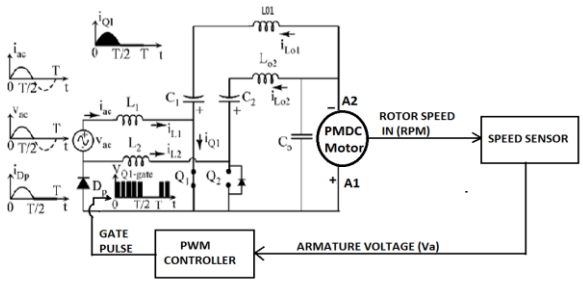
D. Capacitor Selection

The energy transfer capacitors C1 and C2 are important elements in the proposed Cuk topologies since their values greatly influence the quality of input line current. Capacitors C1 and C2 must be chosen such that their steady-state voltages follow the shape of the rectified input ac line voltage waveform plus the output voltage with minimum switching voltage ripple as possible .Also, the values of C1 and C2 should not cause low-frequency oscillations with the converter inductors. In a practical design,the energy transfer capacitors C1 and C2 are determined based on inductors L1 , Lo values (assuming L1 = L2 and Lo 1 = Lo 2 = Lo) such that the resonant frequency (fr) during DCM stage is higher than the line frequency(fl)and well below the switching frequency fs.Thus

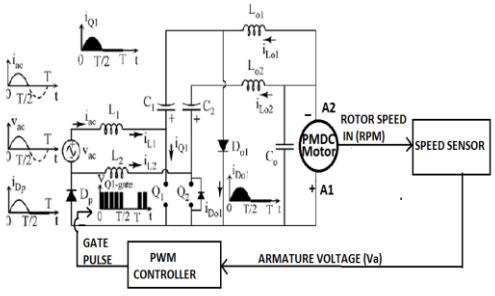
$$f1 < fr < fs \qquad (7)$$

Where $$fr = \frac{1}{2\pi\sqrt{C1(L1+L0)}} \qquad (8)$$

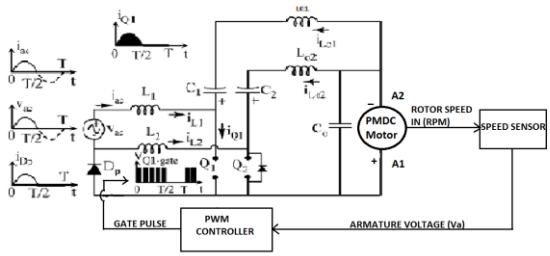
On the other hand, the output capacitor Co needs to be sufficiently large to store minimum energy required for balancing the difference between the time varying input power and constant load power.



(a)



(b)



(c)

Fig.4. Topological stages over one switching period Ts for the converter of Fig.3. Fig.4(a) Switch Q1 is ON.Fig.4(b) Switch Q1 is OFF.Fig.4(c)DCM.

IV.SIMULATION CIRCUITS AND ITS RESULTS

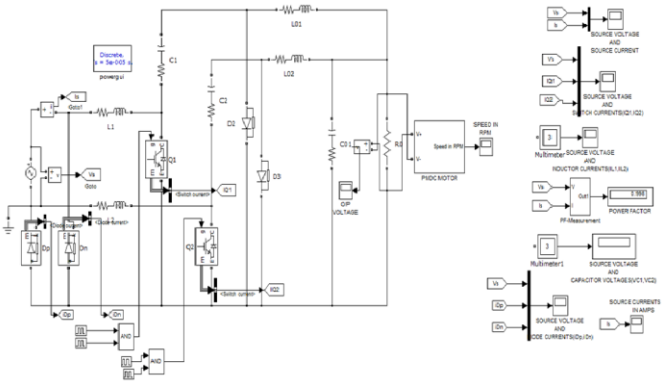


Fig.5.Simulation diagram of bridgeless PFC Cuk rectifier.

The proposed bridgeless PFC Cuk topology has been simulated using MATLAB for the following input and output data specifications: Vac = 120 , Vo = 12V, Pout = 18W, and fs = 50 kHz.Fig.6(a) shows the simulated power factor curve of bridgeless cuk converter. Fig. 6(b) shows the simulated input voltage and current waveforms which are in phase at each other during the full-load condition. Fig. 6(c) shows source voltage & diode current. Fig.6(d) shows current through IGBT switch Q1 and Q2.Fig.6(e) shows current through the inductor L1 and L2. Fig. 6(f) shows voltage through the energy transfer capacitor. Fig. 6(g), which shows the analysis of THD values for the input line current waveform with consideration of number of line current cycles from one to eight .

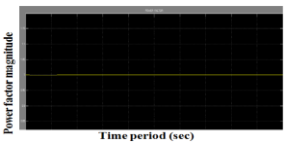


Fig.6 (a) Unity power factor curve of bridgeless cuk converter

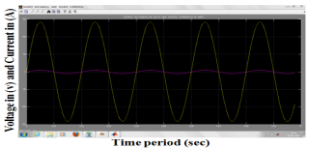


Fig.6 (b) Source voltage and source current of bridgeless cuk converter

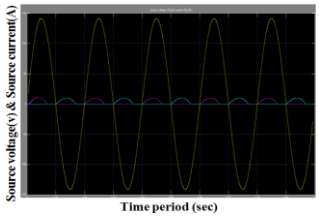


Fig.6 (c) Source voltage and diode current of bridgeless cuk converter

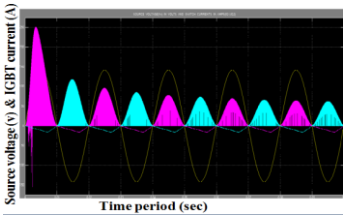
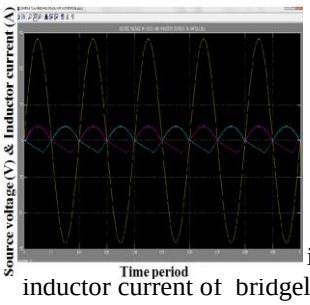
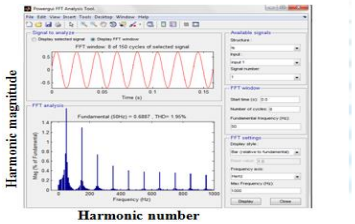


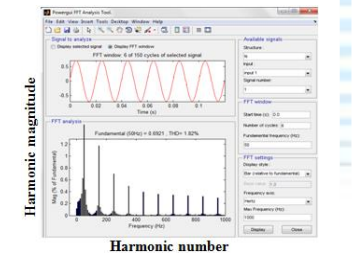
Fig.6 (d) Source voltage and IGBT current of bridgeless cuk converter



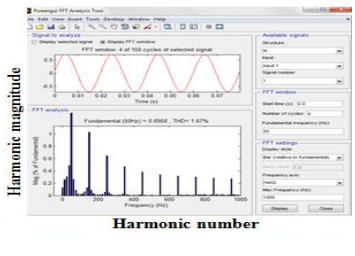
input inductor current of bridgeless cuk converter



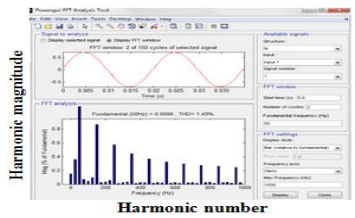
No of cycle =8, THD = 1.95%



No of cycle =6,THD = 1.82%



No of cycle =4, THD = 1.67%



No of cycle =2, THD = 1.49%

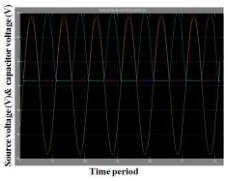
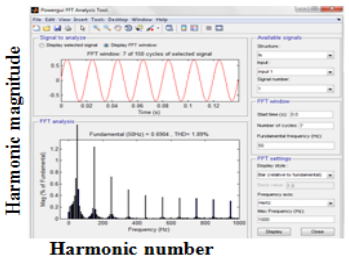
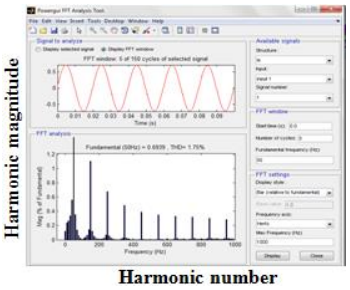


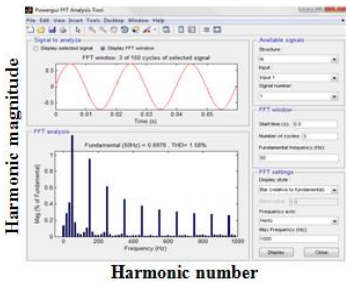
Fig.6 (f) Source voltage and energy transfer capacitor voltage of bridgeless cuk converter



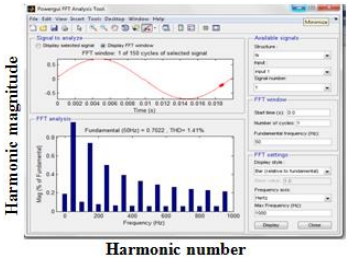
No of cycle =7, THD = 1.89%



No of cycle =5, THD = 1.75%



No of cycle =3,THD = 1.58%



No of cycle =1, THD = 1.41%

Fig.6 (g).THD Analysis for input line current waveform up to eight numbers of cycles

V. CONCLUSION

The proposed single-phase ac–dc bridgeless rectifiers based on Cuk topology are presented and discussed in this paper. The validity and performance of the proposed topologies are verified by simulation results. Due to the lower conduction and switching losses, the proposed topologies can further improve the conversion efficiency when compared with the conventional Cuk PFC rectifier. Namely, to maintain the same efficiency, the proposed circuits can operate with a higher switching frequency. Thus, additional reduction in the size of the PFC inductor and EMI filter could be achieved. The proposed bridgeless topologies can improve the efficiency by approximately 1.4% compared to the conventional PFC Cuk rectifier. The performance of bridgeless types cuk rectifier of the proposed topologies was verified on a 18W PMDC motor in MATLAB circuit. The measured efficiency of the bridgeless cuk rectifier at 120 Vrms line and full load is above 93% with THD below 2%.

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